### Direct Conversion Receiver

# DC Offset and AGC I/Q Imbalance

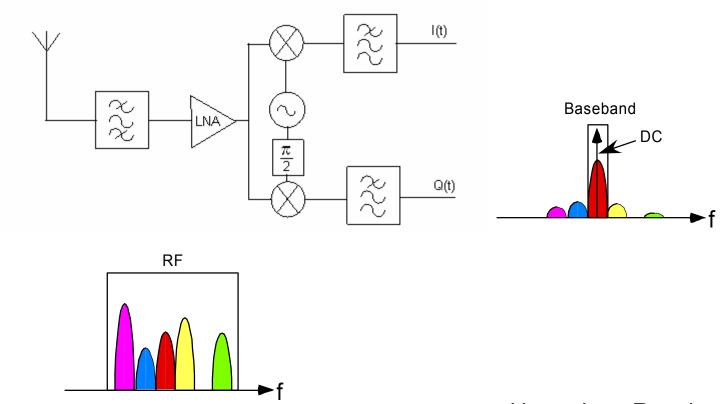
Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.3 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is attached entitled "GNU Free Documentation License".



#### Silicon DSP Corporation

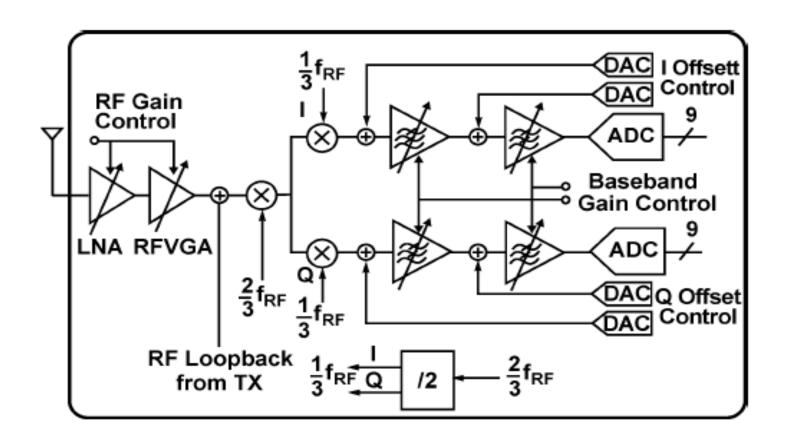
© 2007 Silicon DSP Corporation, All Rights Reserved

### **Direct Conversion Receiver**

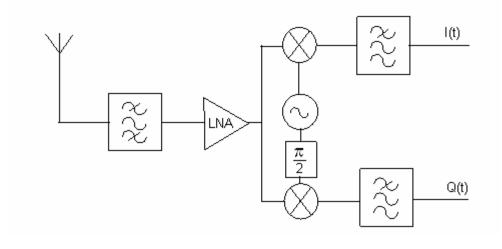


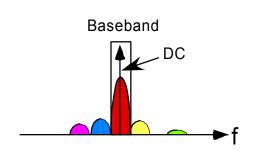
Homodyne Receiver

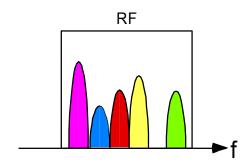
# Heterodyne Receiver



### **Direct Conversion Receiver**

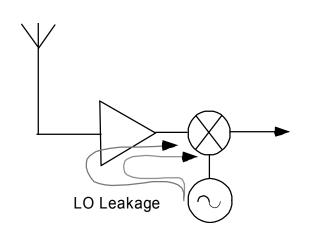


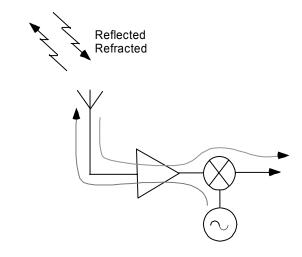


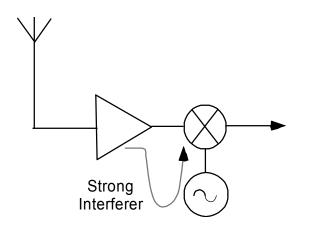


Homodyne Receiver

#### DC Offset Mechanisms





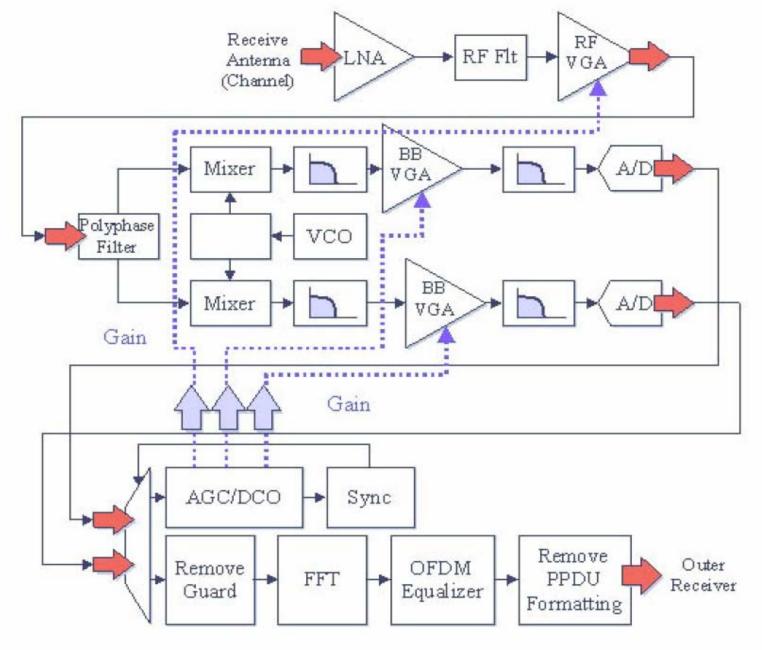


$$\overbrace{\cos 2\pi f_c t}^{\rm LO}(\underbrace{\alpha\cos 2\pi f_c t}) = \frac{1}{2}\alpha(1+\cos 4\pi f_c t)$$

$$DC = \frac{1}{2}\alpha$$

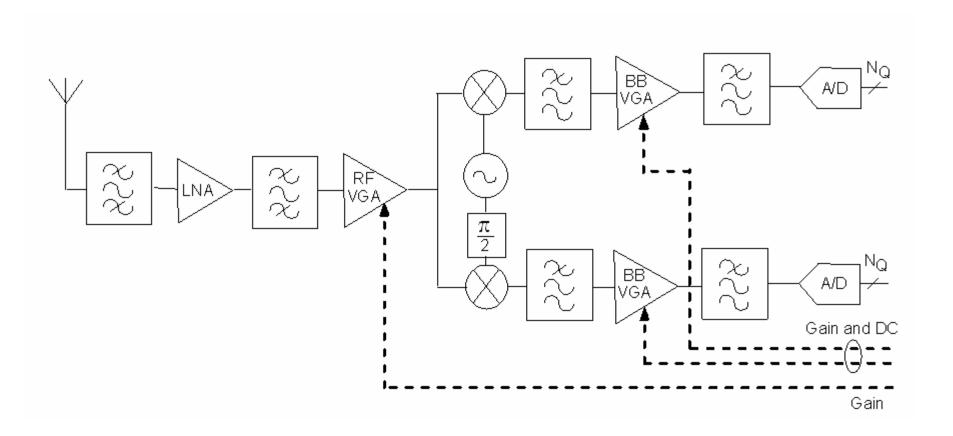
### **Automatic Gain Control**

**Direct Conversion Receiver** 



#### Reference:

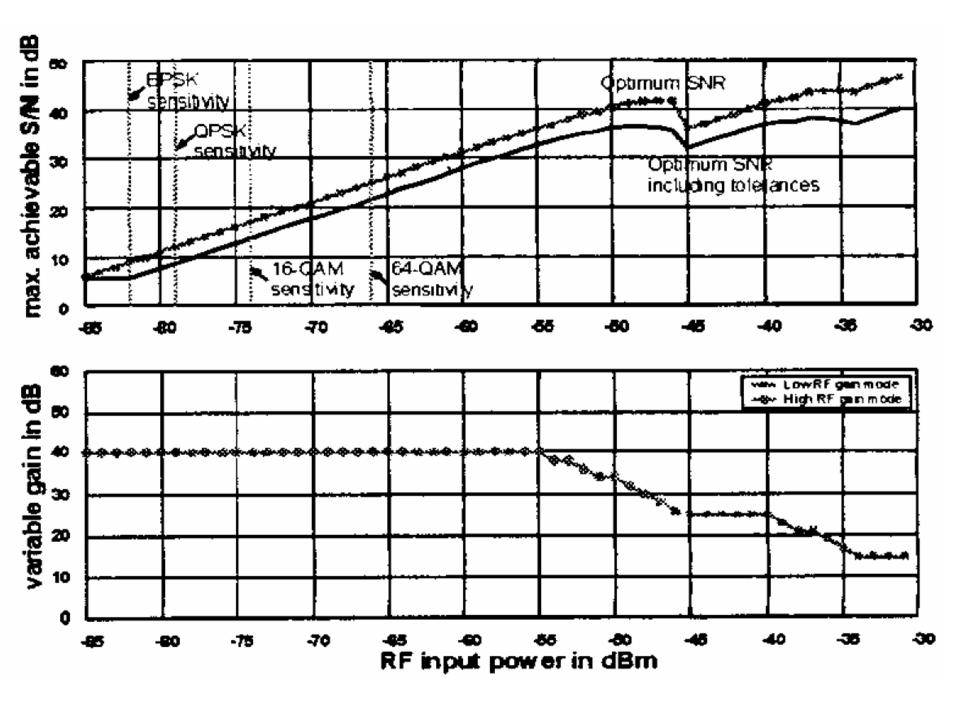
#### **AGC**

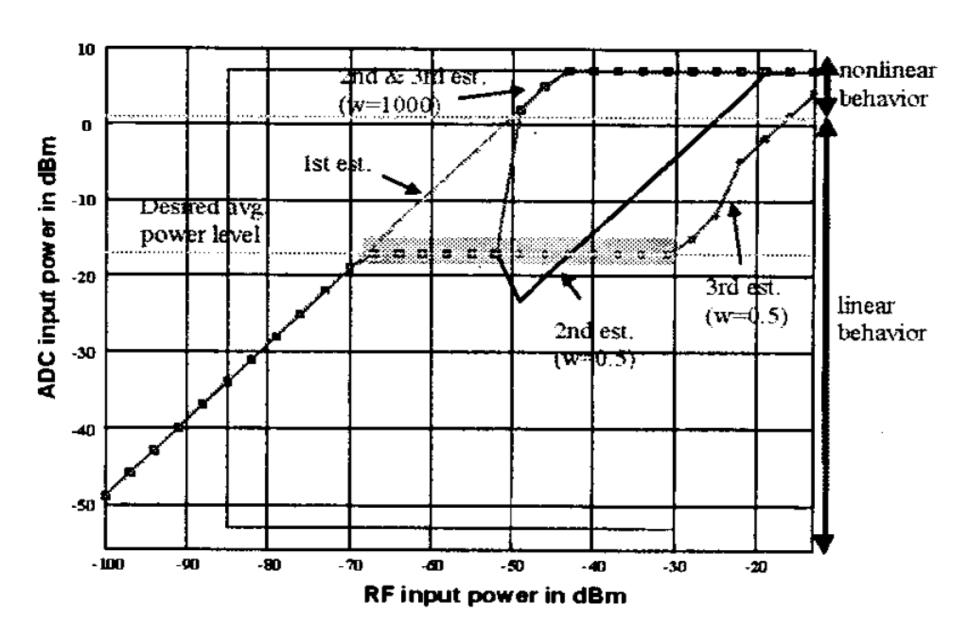


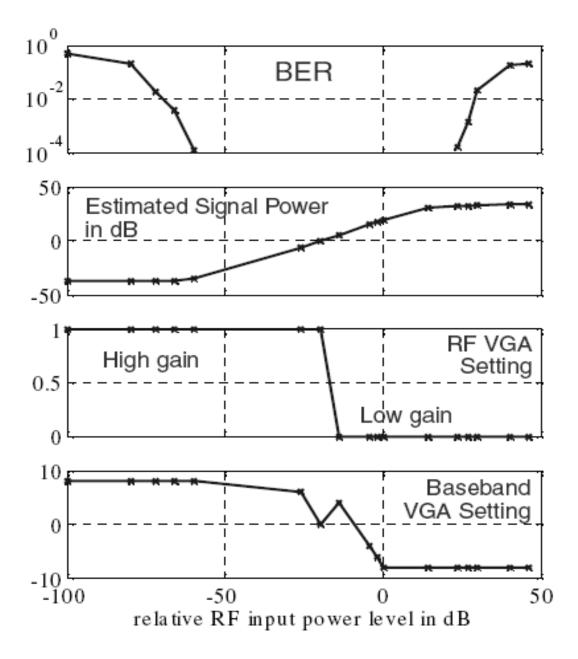
Baseband VGA: -8 to +8 dB gain range in 2 dB steps

#### Reference:

OFDM-WLAN Receiver Performance Improvement using Digital Compensation Techniques Wolgang Eberle, Jan Tubbax, Boris Come, Stephane Donnay, Hugo De Man, Georges Gielen, IMEC and KU Leuven, IEEE, 2002

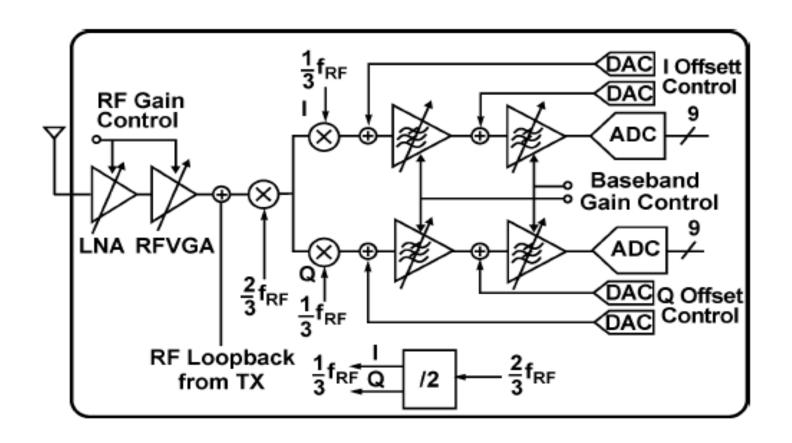




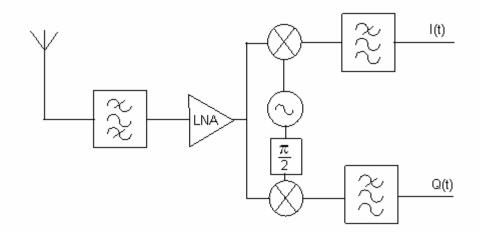


"Behavioral Modeling and Simulation of a Mixed Analog/Digital Automatic Gain Control Loop in a 5 GHz WLAN Receiver" Wolfgang Eberle,, Gerd Vandersteen, Piet Wambacq, Stéphane Donnay, Georges Gielen, Hugo De Man, IMEC, *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition*, 2003

## DC Compensation



#### I/Q Mismatch

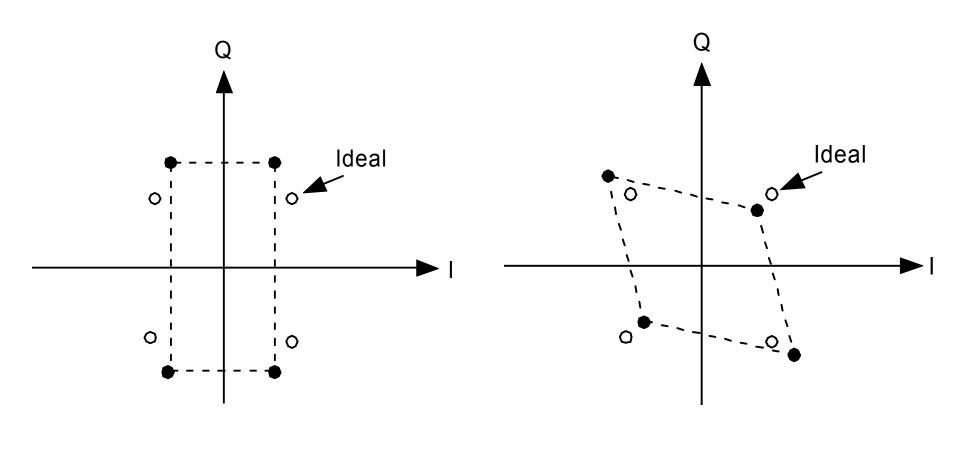


$$x_{LO,I}(t) = 2(1 + \frac{\epsilon}{2})\cos(\omega_c t + \frac{\theta}{2})$$

$$x_{LO,Q}(t) = 2(1 - \frac{\epsilon}{2})\sin(\omega_c t - \frac{\theta}{2})$$

$$x_{BB,I}(t) = a(1 + \frac{\epsilon}{2})\cos\frac{\theta}{2} - b(1 + \frac{\epsilon}{2})\sin\frac{\theta}{2}$$
$$x_{BB,Q}(t) = -a(1 - \frac{\epsilon}{2})\sin\frac{\theta}{2} + b(1 - \frac{\epsilon}{2})\cos\frac{\theta}{2}$$





Phase Error

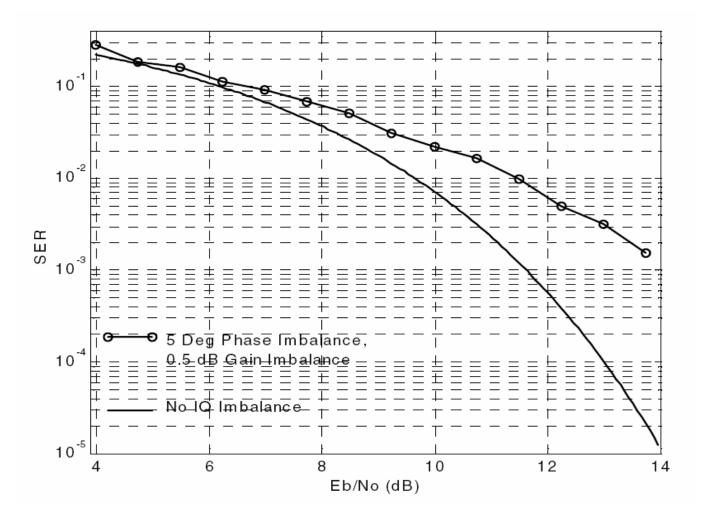
RF Microelectronics, Behzad Razavi, Prentice Hall, 1998

Gain Error

$$\hat{y}_{i}[n] \xrightarrow{\qquad} \widetilde{y}_{i}[n]$$

$$g = \frac{1}{(1+\hat{\epsilon})\cos\hat{\theta}}$$

$$\hat{y}_{q}[n] \xrightarrow{\qquad} \widetilde{y}_{q}[n]$$



SER: Symbol Error Rate "Calibration of IQ Imbalance in OFDM Transceivers", H. Shafiee, S. Fouladifard, 2003 IEEE

TABLE I SUMMARY OF TRANSCEIVER PERFORMANCE

	Measured	Unit
Frequency Band	5.15 – 5.35	GHz
RX NF	4	dB
RX Sensitivity (6Mbps)	$-93.7 \pm 0.9$	dBm
RX Sensitivity (54Mbps)	-73.9 ± 1.2	dBm
RX IIP3	-4.8	dBm
RX IIP2	> 30	dBm
RX Gain Range	15 to 93	dB
TX Power Range	-30 to +18.7	dBm
TX Psat	+23	dBm
TX P-1dB	+19	dBm
Vdd	1.8	V
Vdd_PA	3.3	V
Phase Noise @ 30KHz	-100	dBc/Hz
RX Power Consumption	150	mW
TX Power Consumption	380 (15dBm OFDM output)	mW
ESD	> ±2.5 on all pins	KV
Technology	0.18um 1P5M CMOS	
Die Size	11.7 (including padring)	mm <sup>2</sup>

